TWO-STAGE ANNEALING METHOD FOR MANUFACTURING SEMICONDUCTOR SUBSTRATES

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BACKGROUND ART

The present invention relates to a method for manufacturing semiconductor structures of heterogeneous, non-heterogeneous or homogenous materials and in particular, for silicon containing or silicon-on-insulator ("SOI") structures. The method includes thermally annealing a source-handle-structure by using first and second annealing steps. The first annealing step is stopped before detachment of the source substrate, and the second annealing step is then performed at a lower temperature than the first annealing step to prepare the source substrate for detachment of a useful layer at the predetermined detachment area.

Heterogeneous material compounds or structures such as heterostructures, particularly those consisting of a thin layer of a semiconductor material attached to a handle substrate, have attained considerable industry attention as the next generation of micro-device wafers, especially as used in the fields of microelectronics, optoelectronics or micromechanics.

In semiconductor technologies, thin layers are required which are only a few nanometers to a few micrometers thick with a very low thickness variance. Further, there is a major interest in monocrystalline thin layers. A very suitable technique to produce such thin films on a handle substrate is the SMART-CUT® process, offering a favorable way to produce for instance SOI (silicon on insulator) wafers with a high quality at low cost. One process flow to obtain SOI wafers using the SMART-CUT® process is shown schematically in Figures 6 and 7.

As shown in Figure 6, two starting wafers, for instance a source or top silicon wafer 1' and a handle or base silicon wafer 2', are provided. An implantation of gaseous species like hydrogen and/or a rare gas such as helium is then executed to form a predetermined detachment zone 5' at a certain depth d of the top silicon wafer 1'. Instead of an implantation, any other kind of process can be used which is able to introduce the gaseous species into the wafer 1'.

The predetermined detachment zone defines the location within the top wafer 1' where detachment may occur. After implantation, the top wafer 1' is divided in two regions: a thin

region 3' whose thickness is determined by the used implantation energy, and the remainder 4' of the top wafer 1'.

In the next step, the thin region 3' of the top wafer 1' is bonded on its implanted surface to the base wafer 2'. Bonding is preferentially achieved by so-called direct wafer bonding based on molecular adhesion; however other bonding techniques such as a method with an intermediate glue layer, anodic bonding or a method with electrostatic treatment assistance can be used instead.

As shown in Figure 7, the bonded wafer structure of the wafers 1' and 2' is then heated in a furnace 7 to supply energy to the bonded wafer structure, especially to the implanted wafer 1' which includes detachment zone 5' to weaken the structure. A fracture of the source wafer 1' occurs after applying a certain energy to the wafer structure corresponding to a thermal detachment budget wherein a thermal budget is a certain quantity of energy fixed by two parameters: annealing time and annealing temperature. The fracture can be initiated not only thermally, but also by any form of additional energy brought to the wafer compound, such as mechanical energy or acoustic energy.

The thermal detachment budget is a certain thermal budget corresponding to the limit for thermal detaching or cleaving of a material, which is 100% of the necessary energy at which detachment occurs thermally. The temperature-time-dependency of the thermal detachment budget follows Arrhenius Law in which the reciprocal of the annealing time is proportional to the exponent of the reciprocal of the annealing temperature. The budget of thermal detachment of heterogeneous bonded structures is dependent on a number of material, environmental and technological parameters such as the type of material, implantation conditions and bonding conditions.

Then, the remainder 4' of the top wafer 1' can be detached resulting in a SOI-structure 8' having the thin monocrystalline silicon layer 3' transferred onto the silicon base wafer 2'.

According to the above example, both the top wafer 1' and the base wafer 2' are of silicon. When bonded and subsequently heated, almost no stress is created in the wafers.

Heterogeneous bonded structures such as SOQ (silicon on fused silica) compounds or other structures cannot be annealed at such high temperatures as silicon-oxide-silicon compounds to detach the semiconductor material. The difference between the thermal expansion coefficients of e.g. silicon and fused silica and the different temperature dependencies of the thermal expansion coefficients cause, especially during an annealing step, a high thermal stress in the structure.

In non-implanted bonded heterogeneous wafer compounds this stress leads either to an uncontrolled breakage of at least one of the two wafers and/or to a de-bonding of the wafers. When at least one wafer of the heterogeneous bonded wafer compound is implanted such as in the SMART-CUT® process, there is a sudden variation of stress in the heterogeneous wafer structure after the detachment of a remaining part of the implanted wafer when the detachment occurs at a temperature different from the bonding temperature. This can lead to an indefinite breakage of the wafer compound after such a detachment.

To solve this problem, the temperature of the thermal treatment of the heterogeneous wafer structure can be lowered. However, this lowering of temperature must be significant to avoid any indefinite breakage resulting in very long corresponding annealing times in order to achieve the thermal budget necessary for detachment of the implanted wafer. These annealing times are in the range of several days, and are therefore too long for commercial purposes.

Another solution, which has been presented for instance by Aspar et al in the Proceedings of MRS, 1998, uses a high dose hydrogen implantation to facilitate detachment of a wafer of a heterogeneous wafer compound at the implanted area. However, this high dose ion implantation is expensive.

U.S. Patent No. 6,335,258 describes a method to transfer a thin layer to a heterostructure in which an implanted substrate is thinned down after bonding of this substrate with another substrate to limit a sudden stress variation during detachment of the compound. This method uses an additional processing step and results in significant material consumption because the removed material is lost.

U.S. Patent No. 6,020,252 discloses a method to detach a structure at lower temperatures using a combination of a heat treatment and mechanical efforts such as traction, shearing or bending forces. Such forces can be applied with a tool, a fluid or with another source of mechanical energy, for instance, with a jet as described in U.S. Patent No. 6,427,748.

U.S. Patent No. 5,877,070 suggests two specific methods of a SMART-CUT® process to lower a detachment temperature. The first method is based on an additional boron implantation step of the wafer. This method results in disadvantageous boron doping of the surrounding layers and, especially due to the additional implantation step for boron, is expensive and time-consuming. The second method which is of the above-mentioned type, uses pre-annealing before bonding of the wafers. However, the pre-annealing temperature is

limited by the effect of blistering of the implanted wafer, resulting in a very fast formation of blisters at the surface of the wafer due to thermal treatment. Blistering occurs quickly with annealing and destroys the flatness of the wafer which is necessary for sufficient bonding of the wafer. After bonding, a second annealing step is done at a low temperature. Due to the limited thermal budget applied during the pre-annealing step, the second annealing step takes several days to reach the thermal budget to detach the implanted wafer.

There is a need for a method which can be easily practiced that has a reduced processing time and a very low risk of damage or destruction of the material while still achieving a high quality detached surface. The present invention now satisfies that need.

SUMMARY OF THE INVENTION

The present invention relates to a method for manufacturing a semiconductor structure comprising providing a predetermined detachment area in a source substrate of a first material; bonding the source substrate to a handle substrate of a second material to form a source-handle-structure; annealing the source-handle-structure in multiple annealing steps. The annealing advantageously includes a first annealing step conducted at a first energy level which is lower than the energy of a thermal detachment budget, and a second annealing step conducted at a second energy level that is lower than the first energy level to at least prepare at least the source substrate for detachment of a useful layer at the predetermined detachment area in order to obtain a layer of first material supported by handle substrate.

The useful layer can be detached at the predetermined detachment area by providing additional energy to the source substrate. The additional energy can be thermal energy provided by further heating of the source substrate, or mechanical energy applied to or near the predetermined detachment area of the source substrate. Acoustic energy can also be used, if desired. Also, the second annealing step may be conducted until detachment occurs at the predetermined detachment area to provide the useful layer on the handle substrate.

The first annealing step is typically conducted to provide a substantial portion of the thermal detachment budget. Generally, the first annealing step includes heating to a temperature of about 350°C to 500°C for about a few minutes to about a few hours, and the second annealing step includes heating to a temperature of about 150°C to 350°C for about a few hours to about a few days. Preferably, the temperature of the first annealing step is at least 25% greater than that of the second annealing step, and the second annealing step is conducted for at least twice as long as the first annealing step.

The source-handle-structure may be cooled between the first and second annealing steps, either to a temperature of between about 18°C and 25°C or to the temperature of the second annealing step. The first annealing step may include step-wise heating or cooling to gradually increase or decrease heating temperature. An advantage of stepwise heating in the first annealing step is that it increases the time necessary to complete that step but decreases the time necessary to complete the second annealing step. The first annealing step can include heating to a maximum temperature followed by step wise cooling to lower temperatures.

The predetermined detachment area is preferably made by implantation of hydrogen or rare gas ions to form a zone of weakness that corresponds to the detachment area. Advantageously, the predetermined detachment area is made by implantation of hydrogen ions, helium ions or a combination of hydrogen and helium ions. After annealing, the layer of first material and handle structure is cooled to room temperature for further processing. The source substrate may or may not be cooled, as desired, and is generally re-used.

The second material of the handle substrate generally is different from the first material of the source substrate. The first and second materials are at least one of silicon, a group (III)-(V) semiconductor, an alloy of a group (III)-(V) semiconductor, silicon germanium, silicon carbide, synthetic quartz or fused silica. The present method can also be used for manufacturing a heterogeneous material structure. Preferably, the first and second materials form or comprise a heterogenous semiconductor structure. For example, the source substrate may be a silicon wafer and the handle substrate a wafer of fused silica or synthetic quartz.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 schematically shows a first annealing step of a method according to a first embodiment of the present invention;

Figure 2 schematically shows a second annealing step of a method according to the first embodiment of the present invention;

Figure 3 shows a temperature-time diagram illustrating the temperature-time course during a method according to the first embodiment of the present invention;

Figure 4 shows a temperature-time diagram illustrating the temperature-time course during a method according to a second embodiment of the present invention;

Figure 5 shows a temperature-time diagram illustrating the temperature-time course during a method according to a third embodiment of the present invention;

Figure 6 schematically shows the process preparation steps of a conventional SMART-CUT® process, including oxidation, implantation and wafer bonding; and

Figure 7 schematically shows an illustrative arrangement of an annealing step used in the conventional SMART-CUT® process of Figure 6.

In Figures 1 to 5 the same reference signs as in Figures 6 to 7 are used to denote similar or equal components and parts.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The present invention teaches a method for manufacturing a heterogeneous material structure. The technique includes forming a predetermined detachment area in a source substrate of a first material; attaching the source substrate to a handle substrate of a second, different material to form a source-handle structure, and thermally annealing the source substrate to induce thermal detachment of the source substrate at the predetermined detachment area. Thermal annealing includes a first annealing step of the source-handle-structure. The first annealing step is stopped before detachment of the source substrate. Also included is a second annealing step of the source-handle-structure, after the first annealing step. The second annealing step is performed at a lower temperature than the first annealing step, and continues at least until thermal detachment of the source substrate at the predetermined detachment area.

During the first annealing step, the first material is pre-weakened thermally but not thermally detached at the predetermined detachment area. When the second annealing step starts, some thermal energy has already been introduced in the first material, and a low temperature will then be applied to further weaken the detachment area to facilitate subsequent thermal detachment of the first material at the predetermined detachment area.

The second annealing step therefore applies a thermal energy to the source-handle-structure at a different thermal energy level than that used in the first annealing step. The source substrate can then be detached thermally with a very low risk of destruction occurring during detachment. Accurate detachment occurs at the predetermined detachment area such as an implanted area. The thermal detachment process also avoids further handling of the source-handle-structure for detachment purposes, and therefore reduces the risk of degradation of the substrates that may occur during mechanically assisted detachment, such as those techniques disclosed in U.S. patents 6,020,252 and 6,427,748.

The annealing temperature of the first annealing step can be increased to a relatively high value, which will then shorten the annealing time of the second annealing step resulting in a reduced process time. Detachment can be achieved in a number of ways with the second annealing step. Advantageously, the second annealing step may be continued until detachment of the source substrate occurs. The low temperature of the second annealing step leads to a gentle thermal detachment of the source materials.

It is also beneficial to initiate detachment after the second annealing step by providing additional energy. This way, the process time of the second annealing step can be reduced. In an especially beneficial embodiment, the additional energy is mechanical energy. It has been shown that mechanical energy which is applied after the second annealing step is very effective in providing a final amount of additional energy to split the source-handle-compound. The amount of mechanical energy to be provided is relatively small due to the pre-weakening or pre-fragilization of the detachment area due to the anneal steps.

In a favorable embodiment, the first annealing step is performed at an energy which is lower than the energy of a thermal detachment budget at which the source-handle structure can be detached. In this manner, the first annealing step utilizes an optimum energy applied to the source-handle-structure, which is less than 100% of the thermal detachment budget. This prevents an unintended breakage of the source-handle-structure from occurring, and induces a thermal energy in the source substrate which is high enough to cause a rapid thermal detachment of the source substrate after the second annealing step.

In a further embodiment, the first annealing step is performed at about 70 to 99 % of the temperature-time-ratio of the thermal detachment budget. This range is particularly suitable to obtain a reduced processing time for detachment in the second annealing step.

When the source-handle-structure is cooled between the first annealing step and the second annealing step, the method can be divided into two different physical steps. The source-handle-structure may be cooled to room temperature between the first and the second annealing steps, preferably to a temperature of about between 18°C and 25°C. Use of room temperature requires no further adjustment and allows the easy handling of the wafers between the first and the second annealing steps. Thus, the temperature between the first and the second annealing steps can be below the temperature of the second annealing step.

Alternatively, the source-handle-compound may be cooled to a temperature of the second annealing step between the first and the second annealing steps. This facilitates a change from the first annealing step to the second annealing step and reduces the processing

time. For example, the temperature can be directly cooled down from the first step temperature level to the second step temperature level.

In another advantageous embodiment, the first annealing step and/or the second annealing step may be reduced in a step-wise manner to the annealing temperature. This makes it possible to reduce the annealing time in the second annealing step to result in increased productivity.

In a yet further embodiment, the first material and/or the second material is at least one of a group of materials consisting of silicon, a group (III)-(V) semiconductor, an alloy of a group (III)-(V) semiconductor, silicon germanium, silicon carbide, synthetic quartz and fused silica. With these materials, heterogeneous material compounds can be manufactured which cover most of the presently required heterostructures, for instance in the microelectronics, in the optoelectronics or in the micromechanics fields. In addition, the process can be used to produce non-heterogeneous material structures such as SOIs.

According to a yet further advantageous variant, the source substrate is a silicon wafer and the handle substrate is a synthetic quartz wafer. By this method so-called SOQ (silicon-on-fused silica) wafers can be produced. The method can be easily carried out with reduced processing time and a very low risk of damage or destruction of the material to achieve a high quality of the detached surface.

Figure 1 schematically shows a first annealing step of a first embodiment. A wafer structure 12 includes bonded wafers 1 and 2 is annealed in a furnace 7 which is heated to an annealing temperature T_0 for an annealing time t_0. Wafer 1 is a source wafer made of silicon while wafer 2 is a handle wafer made of fused silica. In another embodiment, wafers 1 and 2 can be of any other semiconductor, conductor or insulator material used in microelectronics or a similar technical field, such as a group (III)-(V) semiconductor, such as GaAs, InP or GaN, an alloy of a group (III)-(V) semiconductor, silicon germanium, silicon carbide, synthetic quartz and fused silica. Wafer 1 and wafer 2 may be of the same or different materials, as desired for the intended use of the final structures.

Wafer 1 is implanted with hydrogen ions to form a buried, predetermined detachment area 5 having a depth d in wafer 1. The area 5 is shown in Figure 1 from the front side as a line. Helium ions either alone or in combination with hydrogen ions can be used to form the detachment area. Optionally, the detachment area can be produced by an implantation of other ions, such as boron or phosphor, or by a combination of these ions with hydrogen or helium ions. For certain applications, boron ions should be omitted, for example, to avoid boron doping of the surrounding layers. The ions can also be buried in wafer 1, for instance

during wafer manufacturing. The area 5 can also be pre-weakened by a local distortion of the crystal structure or crystallinity of the wafer 1, induced for instance by radiation or a mechanical influence.

Figure 2 schematically shows a second annealing step 22 according to a first embodiment where the wafer structure 12 is placed in another furnace 7' and heated up to an annealing temperature T_1 for an annealing time t_1 at least until detachment of the wafer 1 at the pre-weakened buried detachment area 5. Optionally, to employ the second annealing step, the wafer structure can be left in the first furnace 7.

The resulting heterostructure 8 comprises a thin monocrystalline silicon layer 3 which is attached to the handle wafer 2. The remainder 4 of the wafer 1 can be removed from the heterostructure 8 in one piece.

Figures 3 to 5 show temperature-time-diagrams illustrating the temperature-time-course according to first, second and third embodiments of the present method. In the embodiments the following process conditions are used:

Source substrate:	silicon
Handle substrate:	fused silica or silicon
Thickness of buried oxide:	about 50 nm to about 1000 nm
Energy of implantation:	about 30 keV to about 200 keV
Dose of implantation:	about 1×10^{16} cm^{-2} to about 1×10^{17} cm^{-2}

Process window of the first annealing step: between about 350°C to about 500°C, for about a few minutes to about a few hours

Process window of the second annealing step: between about 150°C to about 350°C, for about a few hours to about a few days

Figure 3 shows a temperature-time diagram illustrating the temperature-time course during a method according to a first embodiment in which the temperature is held constant for a period of time during the second annealing step. As shown in Figure 3, the wafer compound 12 is introduced into the furnace 7 at a room temperature T_R during the first annealing step 21. The room temperature T_R corresponds to a temperature value between about 18° and 25°C. The temperature is then continuously increased up to the annealing temperature T_0, which is about 425°C in the example shown. The temperature is then held at the level of T_0 for several minutes. Alternatively, the temperature can be held constant for a longer period of time, such as several hours. Thereafter, the temperature is continuously cooled down to room temperature T_R.

In another embodiment, the wafer compound 12 can be introduced into the furnace 7 at different temperatures. The temperature of the furnace 7 can be modified in accordance with the type of furnace and the implantation conditions.

The energy applied to the heterogeneous bonded wafer structure 12 in the first annealing step 21 corresponds to about 90% of the detachment thermal budget of the wafer compound 12 that would result in detachment. The first annealing step 21 causes weakening at the predetermined detachment area, but without detachment of the wafer 1 from the wafer 2 and without affecting the bond of the wafer-compound 12.

In a second annealing step 22, the wafer compound 12 is heated to a temperature T_1 and is then held at this temperature for a longer period of time t1, for example about 1800 minutes. At an annealing time and an annealing temperature which is marked by the arrow H, the wafer structure thermally detaches. Thereafter, the detached wafer parts are cooled down to room temperature T_R.

Figure 4 shows a temperature-time diagram illustrating the temperature-time course according to a second embodiment of the present method in which the temperature is cooled after a first annealing step 21' directly to the temperature T_1 of the second annealing step 22.

Figure 5 shows a temperature-time diagram illustrating the temperature-time course according to a third embodiment of the present method in which the temperature is reduced in a step-wise manner during the first annealing step. In the third embodiment, the wafer structure 12 is heated in the first annealing step 21 from room temperature T_R to a value T_0, is further held constant at this temperature T_0 of about 425°C for several minutes, and is then cooled over several temperature steps T_2,T_3,T_4 down to room temperature T_R. In the example shown, the wafer structure 12 is first cooled to a temperature T_2 which is about 20° to 30° lower than temperature T_0. The wafer structure 12 is held constant at this temperature T_2 for a couple of minutes. Thereafter, the wafer structure 12 is cooled down to a temperature T_3 which is an additional 20° to 30° lower than temperature T_2. After a few minutes, the wafer compound is further continuously cooled down to a temperature T_4 of about 350°C where it is held constant for several minutes and is then cooled down to room temperature T_R.

The energy applied to the wafer structure 12 during the first annealing step 21 corresponds to about 90% of the thermal detachment budget of the wafer compound 12 that would result in detachment.

In the second annealing step 23, which follows the first annealing step 21, the wafer structure 12 is heated from room temperature T_R to a temperature T_5 of about 300°C where it is held constant for about 60 to 80 minutes until detachment occurs. The energy applied to

the wafer structure in the second annealing step 23 corresponds to about 10% of the thermal detachment budget. The detachment point is marked with an arrow E.

In another embodiment of the invention (not shown), the second annealing step 23 can be stopped before detachment occurs. Then, an additional amount of energy is applied to the wafer compound 12. The additional energy may be provided in any form, such as mechanical energy, radiation or acoustic energy, which leads to splitting of the wafer compound 12. This energy is much less than that which would otherwise be needed if the two annealing steps were not conducted.

After detachment, the heterostructure 8 and the remainder 4 of the source wafer 1 generally are cooled down to room temperature T_R.

As indicated by dotted line 3'in Figure 5, in another embodiment, the wafer structure 12 can be held constant at the temperature T_5 for longer than 80 minutes, even up to about 160 to 200 minutes. In Figure 5, the subsequent steps in which the temperature is reduced in a stepwise manner enables a reduction of the duration of the last step where thermal detachment occurs. This variant optimizes the pre-weakening step. It can be applied to the first and/or the second annealing steps 21, 23.

In the following, the function and the effect of the embodiments shown are explained.

With reference to Figure 3, in the first annealing step 21, a relatively high temperature T_0 is applied for a relatively short time. The annealing temperature and annealing time corresponds to about 90% of the thermal budget of the bonded wafer structure. At a thermal budget T_0, t_0 an initial thermal energy can be applied to the wafer structure, to pre-weaken the pre-determined buried detachment area in the source wafer 1 of the wafer structure, which forms the basis for a later detachment phenomenon. The second annealing step 22 is performed after the first one and at a much lower temperature than that used during the first annealing step 21. The optimization of pre-weakening can occur not only in the first annealing step but also in the second annealing step.

Referring again to Figure 3, the temperature of the first annealing step 21 is about 400°C to 450°C whereas the temperature of the second annealing step 22 is below 400°C. The induced thermal energy during the second annealing step helps to detach the wafer compound into two wafer parts along the predetermined detachment area 5. This results in a SOQ wafer 8 consisting of the quartz substrate 2 and a thin silicon layer 3 thereon or in a SOI wafer consisting of a silicon substrate and a thin silicon layer thereon.

With reference to Figure 4, where nearly the same annealing temperatures and annealing times are used as in the first embodiment shown in Figure 3, the temperature

between the first annealing step 21' and the second annealing step 22 is cooled down to the temperature T_1 of the second annealing step 22. The annealing steps 21', 22 may be performed in the same furnace 7. This shortens the transition time from the first annealing step 21' to the second annealing step 22 and therefore reduces the entire processing time.

As shown in Figure 5, the annealing time of the second annealing step 23 can be shortened by rapidly heating the wafer structure 12 in the first annealing step 21 to a temperature T_0 of about 425°C, and a reducing the temperature in a step-wise manner at certain temperature levels T_2, T_3, T_4. The thermal energy applied to the structure of the wafer structure 12 in the two annealing steps 21, 23 corresponds to 100% of the thermal detachment budget of the wafer structure 12, so that after a certain period of time at the temperature T_5 of the second annealing step 23 thermal detachment of the wafer structure in the area 5 can be achieved.

The stepwise reduction of the temperature in the first annealing step 21 also can lead to a pre-weakening to attain an easier detachment in the second annealing step 23. Instead of the temperature profile shown in Figure 5, any other favorable temperature profile can be used for detachment of the wafer structure 12.

Moreover, it is possible to change the temperature in the first annealing step 21 so that the temperature difference between the temperature steps T_0, T_2, T_3, or T_4 rises. For instance, the temperature can be reduced from T_0 to T_3 and thereafter can be further enhanced to T_2 and then again reduced to T_3 and to T_R.

Furthermore, it is possible to combine the first and the second annealing steps into one annealing step in which the temperature between the two annealing steps is not reduced to room temperature T_R.

It should be further taken into consideration that the above-mentioned annealing times and annealing temperatures are favorably related to detachment of wafer structures consisting of silicon and fused silica with conventional thicknesses, warps and thermal features. When other substrates with other features or different implantation conditions are used, it should be understood that the given times and temperatures are to be adapted accordingly.